Speeding up Router for FPGA CAD

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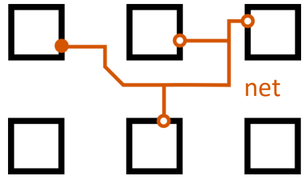
1 - Background

FPGAs – reprogrammable hardware

ALTERA XILINX bing

CAD routing



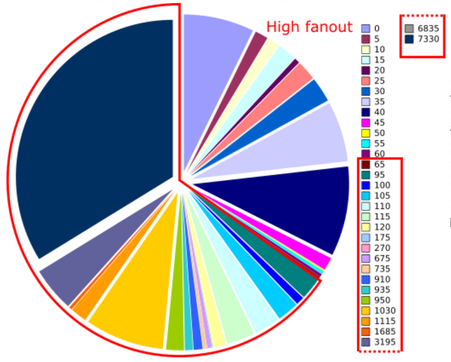
Make the fastest legal circuit possible

2 - Problem

Routing is too slow – commercial tools demonstrate it can be done faster.

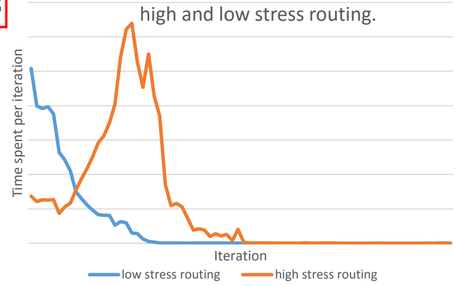
3 - Method

Figure 1. Route time distribution for nets of different fanout



Profile per iteration and per fanout results

Figure 2. Time per iteration profiles for high and low stress routing.

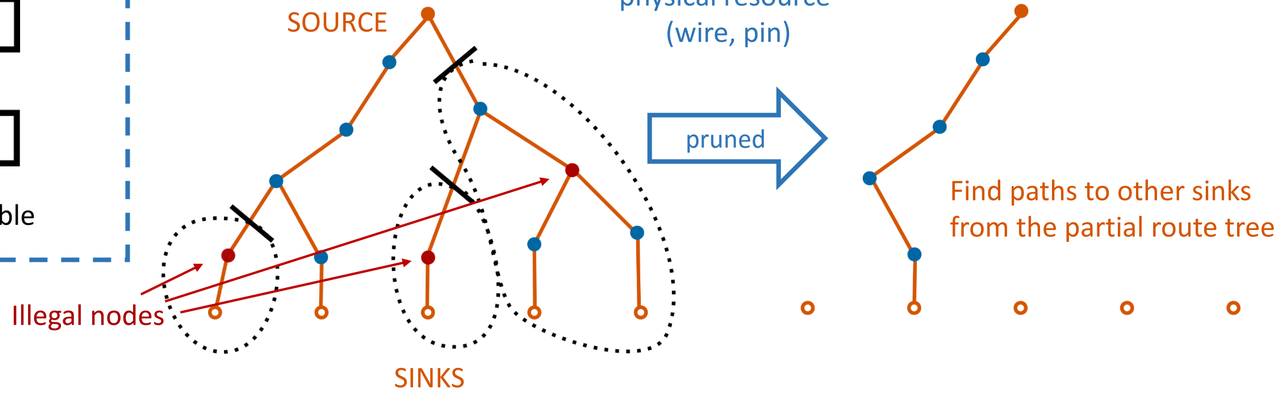


4 - Hypothesis

Speed up can be achieved by reusing previous iteration's routing – iterative rerouting

Route tree pruning

Each node is a physical resource (wire, pin)



5 - Results

Figure 3. Time per iteration comparison on a large Titan benchmark

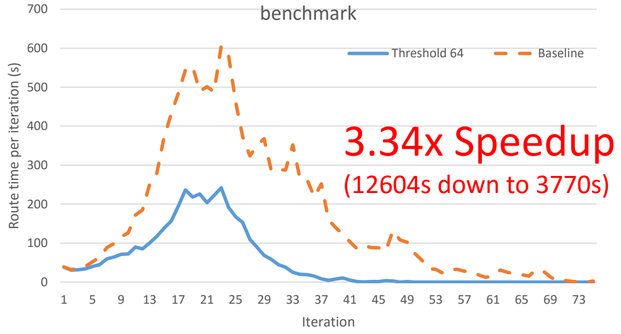


Figure 4. Geometric average route time for large circuits.

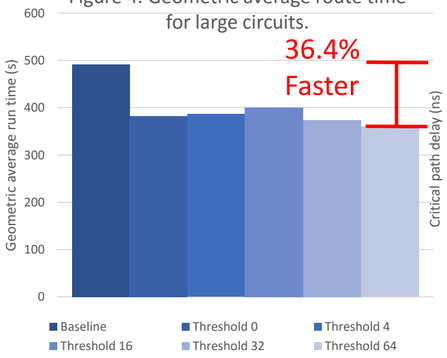
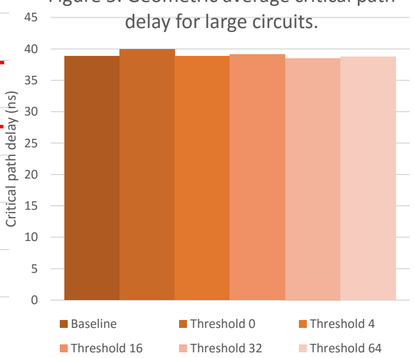


Figure 5. Geometric average critical path delay for large circuits.



6 – Conclusion and future work

- Reduce by reuse
- More effective with larger sized circuit
- Threshold provides stability

- Source-to-sink binning to geometrically limit the nodes looked at

Figure 6. Total route time spent on small circuits for different iterative rerouting thresholds.